Amendments to the Claims

1. (currently amended): A dc/dc converter comprising:

an inductor coupled to one of a positive output terminal and a positive input terminal;

a first depletion mode compound semiconductor switching FET ~~coupled~~ connected to the inductor and configured to control current flow in the inductor;

a control circuit coupled to a gate of the first depletion mode compound semiconductor switching FET for switching the first depletion mode compound semiconductor switching FET between an on state and an off state; and

a capacitor coupled to the positive output terminal and a negative terminal.

2. (currently amended): The dc/dc converter of claim 1 wherein the first depletion mode compound semiconductor switching FET comprises a GaAs n-channel depletion mode junction field effect transistor.

3. (currently amended): The dc/dc converter of claim 1 further comprising a second depletion mode compound semiconductor switching FET coupled to the first depletion mode compound semiconductor FET and the control circuit and configured to control current flow in the inductor.

4. (currently amended): The dc/dc converter of claim 3 1 wherein the second depletion mode compound semiconductor switching FET comprises a GaAs n-channel depletion mode junction field effect transistor.

5. (currently amended): The dc/dc converter of claim 1 further comprising:

a second switching FET device coupled to the negative terminal and the control circuit; and

a diode having a cathode and an anode, wherein the anode is coupled to the negative terminal and the cathode is coupled between the inductor and the first depletion mode compound semiconductor switching FET, and wherein the first depletion mode compound semiconductor switching FET is connected to the positive input terminal, and wherein the inductor is coupled to a source of the first depletion mode compound semiconductor switching FET and the positive output terminal to form a buck converter.

6. (currently amended): The dc/dc converter of claim 5 wherein the second ~~depletion mode compound semiconductor~~ switching FET comprises a depletion mode compound semiconductor switching FET device.

7. (currently amended): The dc/dc converter of claim [[5]] 6 wherein one of the first and second depletion mode compound semiconductor switching FETs comprises a GaAs n-channel depletion mode JFET.

8. (currently amended): The dc/dc converter of claim [[5]] 6 wherein both the first and second depletion mode compound semiconductor switching FETs comprise GaAs n-channel depletion mode JFETs.

9. (currently amended): The dc/dc converter of claim 1 further comprising a second depletion mode compound semiconductor switching FET device coupled to a negative terminal and the control circuit, and wherein the inductor is coupled between the positive input terminal and a drain of the first depletion mode compound semiconductor switching FET device to form a boost converter.

Claim 10 (cancelled).

11. (currently amended): The dc/dc converter of claim [[10]] 9 wherein one of the first and second depletion mode compound semiconductor switching FETs comprises a GaAs n-channel depletion mode junction field effect transistor.

12. (currently amended): The dc/dc converter of claim [[10]] 9 wherein both the first and second depletion mode compound semiconductor swithcing FETs comprise GaAs n-channel depletion mode junction field effect transistors.

13. (currently amended): The dc/dc converter of claim 1 wherein the first depletion mode compound semiconductor switching FET comprises:

a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact;

a first trench formed in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface;

a second trench formed within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface;

a first source region formed in the body of semiconductor material extending from the upper surface and spaced apart from the first trench; and

a doped gate region formed in at least a portion of the second sidewalls and the second bottom surface, wherein the doped gate region comprises a second conductivity type.

14. (original): The device of claim 13 wherein the body of semiconductor material comprises GaAs.

15. (currently amended): A dc/dc converter network comprising:

a first vertical trench gate compound semiconductor depletion mode FET device;

an inductor connected to the first FET device and one of a positive input terminal and a positive output terminal;

a gate control device connected to the first FET device;

a second vertical trench gate compound semiconductor depletion mode FET device connected to a negative terminal, the gate control device and the first vertical trench compound semiconductor depletion mode FET device; and

a capacitor connected to the positive output terminal.

Claim 16 (cancelled).

17. (currently amended): The dc/dc converter network of claim [[16]] 15 wherein one of the first and second vertical trench gate compound semiconductor depletion mode FET devices comprises a GaAs n-channel depletion mode junction field effect transistor.

18. (currently amended): The dc/dc converter network of claim [[16]] 15 wherein the first and second vertical trench gate compound semiconductor depletion mode FET devices comprise GaAs n-channel depletion mode junction field effect transistors.

19. (currently amended): A dc/dc converter circuit including:

an inductor connected to one of a positive input terminal and a positive output terminal;

a first GaAs depletion mode vertical trench gate JFET device connected to the inductor;

a second GaAs depletion mode vertical trench gate JFET device connected to the first JFET device and a negative terminal;

a gate control device connected to the first and second JFET devices; and

a capacitor connected to the positive output terminal and the negative terminal.

20. (currently amended): The dc/dc converter circuit of claim 19 wherein one of the first and second GaAs depletion mode vertical trench gate JFET devices comprises an n-channel device.